

Generation of Triggering Signals for Multilevel Converter

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Abstract

Multilevel converter has become attractive in the power industries and it can be applied in many applications especially on improvement of the power quality. This paper presents the generation of triggering signals used to control the cascaded H-bridge (CHB) multilevel converter. One of the carrier based pulse width modulation scheme which is level shifted multicarrier modulation has been chosen to control the IGBTs in CHB multilevel converter. A simulation circuit of three phases five levels CHB multilevel converter is designed and the triggering signals are observed. Development of a PIC program has been performed to generate the experimental triggering signals using a PIC microcontroller.

Keywords: Multilevel converter cascaded H-bridge, level shifted multicarrier modulation, triggering signals.

1. Introduction

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform [1]. To obtain a low distortion output voltage or a nearly sinusoidal output waveform, a triggering signal should be generated to control the switching frequency of each power semiconductor switch. In this work, the triggering signals of multilevel converter are designed using the carrier based pulse width modulation (PWM) scheme, since the PWM provides high power with low harmonics. A three phase CHB multilevel converter circuit is designed and simulated using the MATLAB SimPowerSystems software. Then, a C-language program is written

according to the triggering signals obtained in the simulation results. The outcomes of this project are merely triggering signals generated using PIC microcontroller.

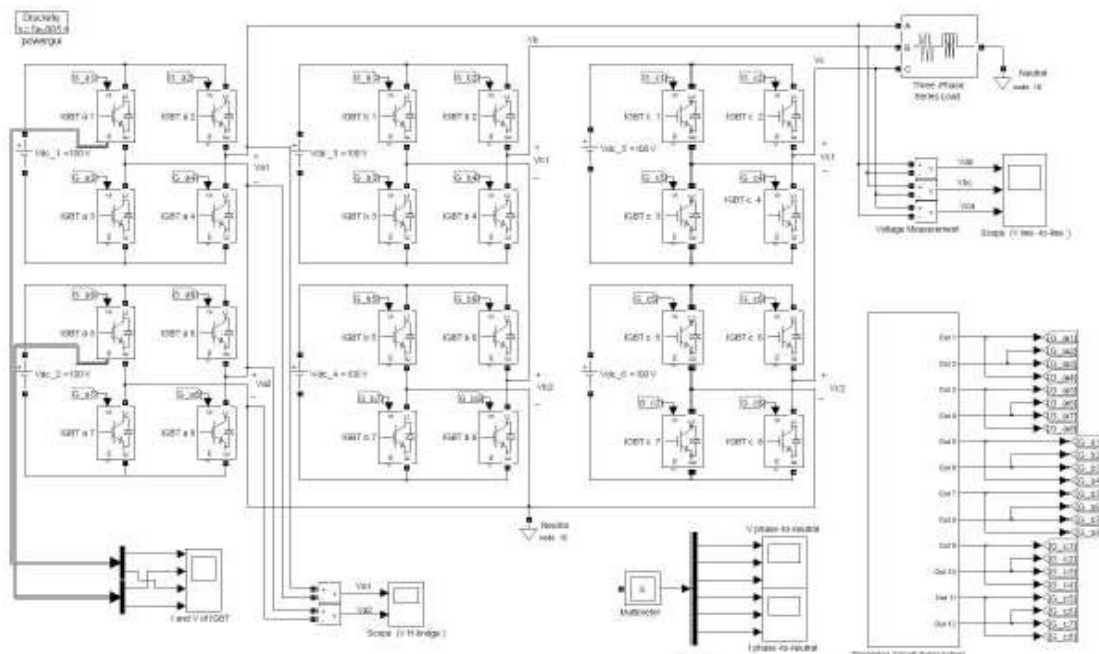
2. Simulation Circuit

A. Three phase Five Levels Cascaded H-bridge Multilevel Converter

This type of CHB multilevel converter has been designed and simulated using MATLAB SimPowerSystems. The multilevel circuit is illustrated in Fig.1. IGBT has been chosen as the power semiconductor switches in each H-bridge, since it has more features than other power semiconductor switches.

The five levels multilevel converter requires two separate dc sources per phase leg, this means that two H-bridge inverters are used for single phase structure.

Figure 1: Three phase five level CHB multilevel converter



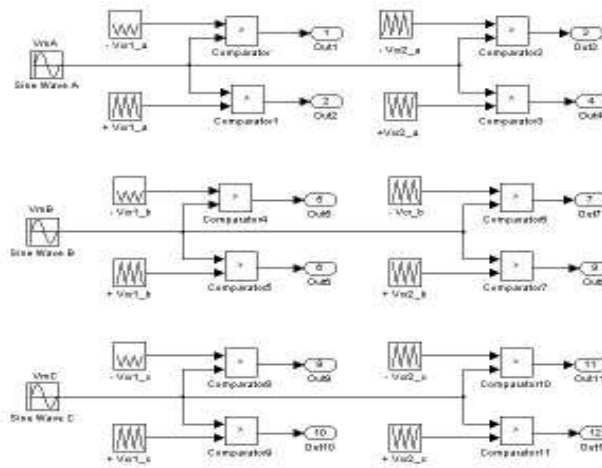
One of the terminals of each single phase five levels CHB multilevel inverter is connected as star, while the other terminal of each single phase CHB multilevel converter is connected to a three phase series load [2]. For experimental lab scale model, the value of nominal phase to phase voltage is 300V, nominal frequency is 50Hz, active power is 3000W, inductive reactive power is 500 Var, in the circuit, and 24 IGBTs were used. Both IGBTs connected in series in half H-bridge can not be turned on at the same time to avoid the shoot through fault. Hence, a twelve pulses triggering circuit is designed to trigger 24 IGBTs to obtain the staircase output voltage. The output triggering signals is shown in Fig. 2.

The triggering circuit is designed based on the three phase sinusoidal modulation waves, V_a , V_b , and V_c . Three of the sine wave sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers wave sources block parameters, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs.

Fig. 3 shows the waveforms based on three schemes of level shifted multilevel modulations: (a) in phase disposition (IPD), where all carriers are in phase; (b) alternative

phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above zero reference are in phase but in opposition with those below the zero reference [3].

Figure 2: Triggering circuit inside the sub



For PID modulation, the multilevel converter with multilevel requires (m1) triangular carriers with same amplitude and frequency. The frequency modulation index m_f which can be expressed as:

$$m_f = \frac{f_{cr}}{f_m} \tag{1}$$

where f_m is modulating frequency and f_{cr} are carrier waves frequency. The amplitude modulation index m_a is defined by

$$m_a = \frac{V_m}{V_{cr} m-1} \quad \text{for } 0 \leq m_a \leq 1 \tag{2}$$

Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of the each carrier wave [3]. The amplitude modulation index, m_a is 1 and the frequency modulation index, m_f is 6.

B. Three Phase Seven Levels Cascaded H-bridge Multilevel Converter

To compare the values in term of total harmonic distortion and output voltage with the three phase five levels CHB multilevel converter and seven levels as shown in Fig. 4. In this case, only APOD level shifted multicarrier modulation is used to compare with five levels CHB multilevel converter. Fig.5 shows the waveform of APOD level shifted multicarrier modulation.

Figure 3: Waveforms based on level shifted multicarrier modulations

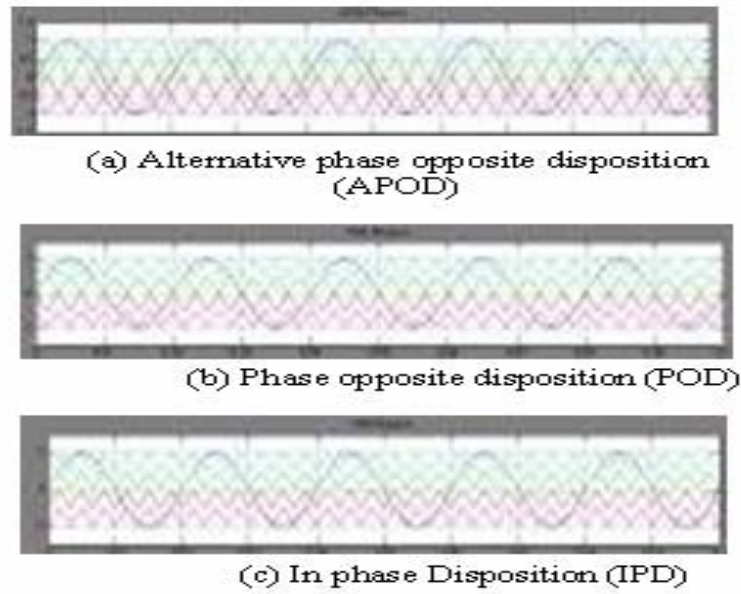


Figure 4: Three phase, seven levels CHB multilevel converter

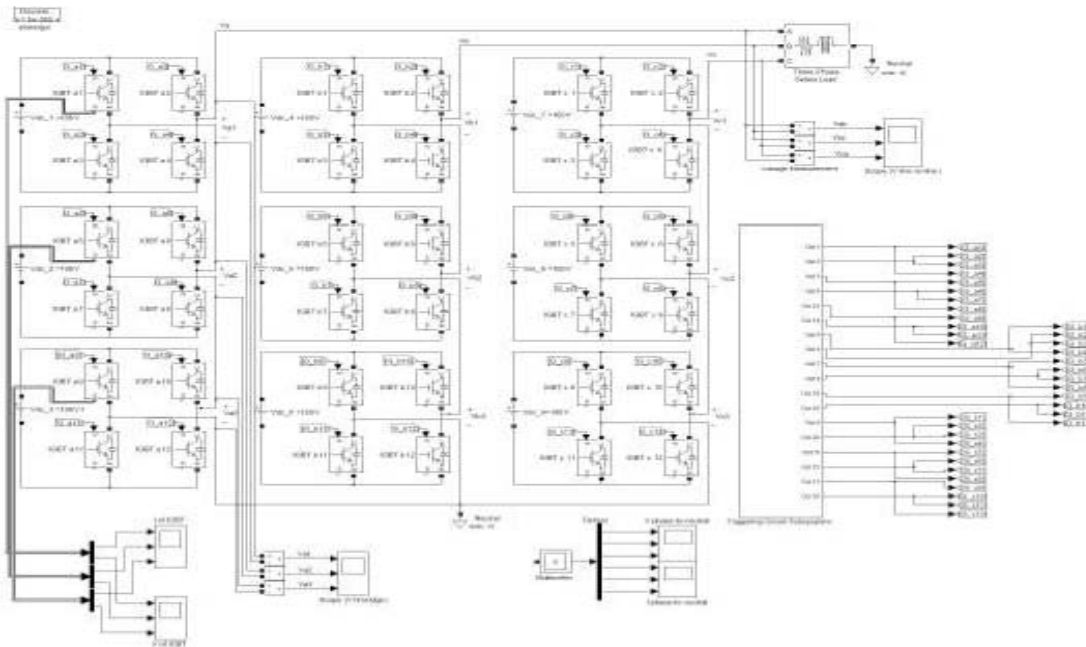
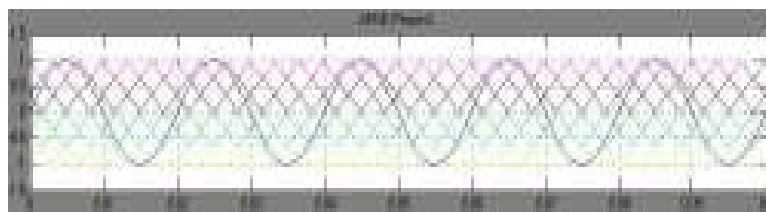


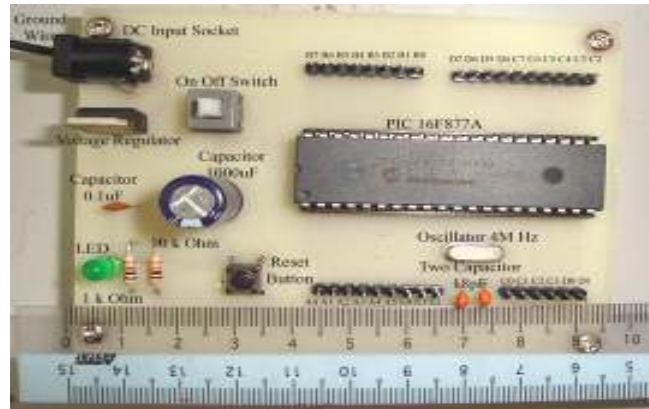
Figure 5: Waveform of APOD level shifted multicarrier modulation



3. Experiment Setup

Fig shows the PIC 16F877A microcontroller which has many features and easy to assembled. This microcontroller has been used to generate the required twelve PWM triggering signals.

Figure 6: Microcontroller PIC 16F877A



4. Results

A three phase five levels CHB multilevel converter circuit shown in Fig 1 has been developed and tested. The voltage across each individual H-bridge, V_{a1} and V_{a2} , V_{an} has been obtained as shown in Fig. 7.

The line to line voltage of CHB multilevel converter using APOD, IPD and POD modulations are shown in figs.7, 8, and 10, respectively.

Figure 7: Voltage of H-bridge V_{a1} and V_{a2} and V_{an} at phase A with APOD modulation.

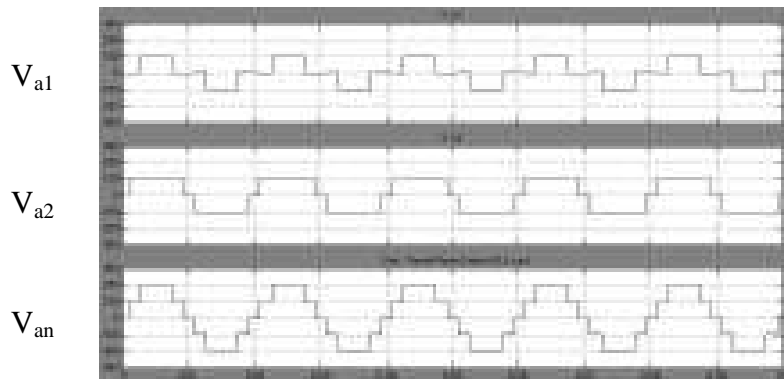


Figure 8: Line-to-line voltages with APOD modulation



Figure 9: Line-to-line voltages with IPD modulation

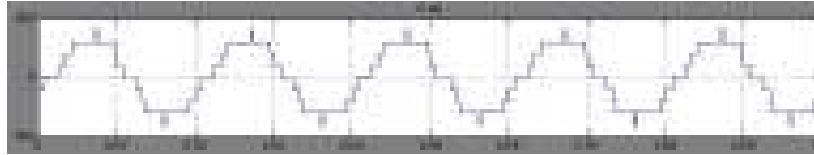


Figure 10: Line-to-line voltage with POD modulation

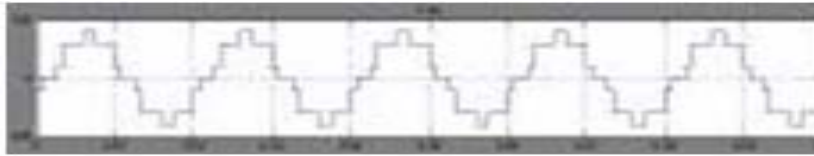


Table 1: Fundamental values and THD using different level shifted multicarrier

	APOD		POD		IPD	
	Fund. (50Hz)	THD (%)	Fund. (50Hz)	THD (%)	Fund. 50Hz)	THD (%)
I_{an}	7.109	7.90	7.251	14.82	6.596	14.85
I_{bn}	6.769	16.78	6.912	20.62	6.240	22.99
I_{cn}	6.819	14.63	6.962	18.87	6.417	19.13
U_{an}	210.4	17.14	214.6	23.87	195.2	23.35
U_{bn}	209.5	18.28	213.8	25.39	193.9	24.71
U_{cn}	209.5	18.24	213.8	25.36	194.3	24.22
V_{ab}	363.4	17.13	370.9	19.64	337.0	17.82
V_{bc}	363.5	17.72	369.9	20.98	336.1	18.96

The differences between the methods of modulation APOD, IPD, and POD can be noticed by calculating the THD of the line to neutral voltages [4]. Table I shows in line to neutral voltage V_{an} and current of phase leg A with term of voltage and current between the IPD. it shows that APOD modulation has lowest values in term of THD among these modulations, followed by POD and IPD.

APOD modulation has been adopted to generate the triggering signals for seven levels CHB. The voltage waveforms at different points of this CHB have been obtained as shown in Figs. 11 to 13. The fundamental values and THD of seven levels CHB multilevel converter is shown in Table II.

Figure 11: Voltages of H-bridge

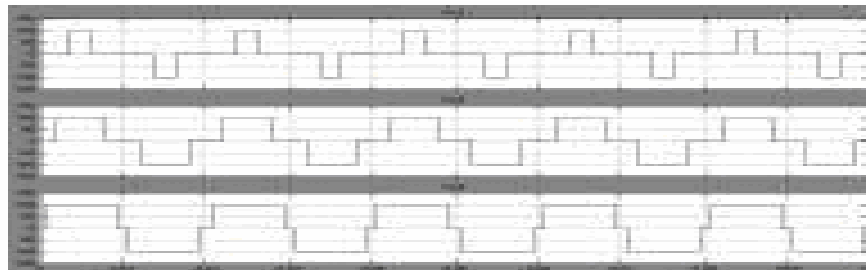


Figure 12: Line-to-neutral voltage

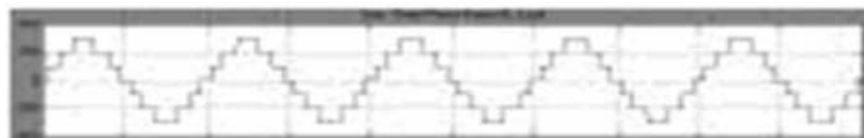


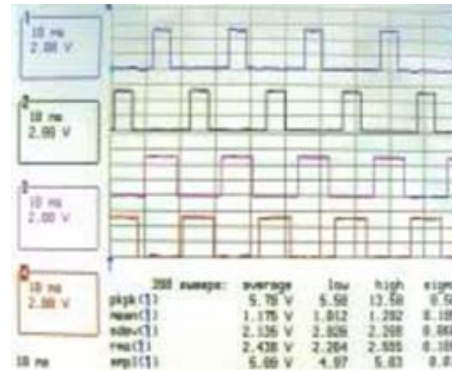
Figure 13: Line-to-line voltage**Table 2:** THD of seven level multilevel CHB

	Fund. (50Hz)	THD (%)
I_{an}	5.805	9.07
I_{bn}	5.543	19.59
I_{cn}	5.613	16.27
U_{an}	275.7	16.39
U_{bn}	275.0	17.46
U_{cn}	275.0	17.43
V_{ab}	476.9	12.98
V_{bc}	476.3	14.39
V_{ca}	476.9	12.94

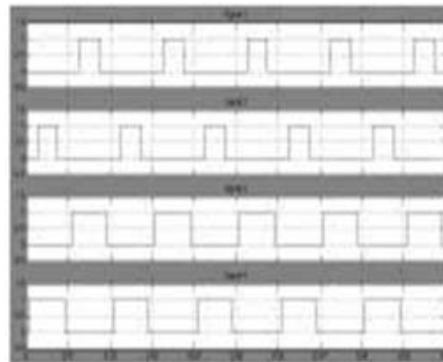
It can be noted that, the THD voltages of the seven level multilevel converter are slightly lower if compare with the five level multilevel converter which using same APOD modulation. That means the voltages can be improved when the level of multilevel are increased. However, the THD currents are slightly higher at seven level converters when compared with the five level multilevel converters. This may due to inefficient modulation applied to that multilevel converter. The line-to-line voltages of seven level CHB converters are more distorted than the five level CHB converters. If a programmed PWM method is used to generate the triggering signals, the quality of voltage and current may be improved. The programmed PWM method is introduced to eliminate the high order harmonics [5].

The simulation triggering signals required for phase leg A is shown in Fig.14, by referring to the Fig. 1, Signal (1) is used to control the IGBTs a_1 and a_4 and Signal (2) used to control the IGBTs a_2 and a_4 , while IGBTs a_5 and a_6 and also IGBTs a_7 and a_8 are controlled by signals 3 and 4 respectively.

A program with C-language has been written to generate the required signals. Only the experimental and simulation triggering signals of phase A is shown since the waveform of other phases triggering signals are similar.

Figure 14: Signals generated by microcontroller

Experimental



Simulation

5. Conclusion

In this work a simulation of three phase five level CHB multilevel converter has been developed and compared with a seven level multilevel converter. Three types of the level shifted PWM multicarrier modulations were considered to generate the PWM triggering signals to control the IGBTs. Among those three modulations, it has been found that, APOD modulation is better than others in term of THD. Therefore, the triggering signals of APOD modulation were chosen and written into the programming. The final outcome of this work is the experimental triggering signals generated by using microcontroller.

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