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Design and FPGA Implementation of High Speed, Low Power Digital Up Converter for Power Line Communication Systems

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Abstract

The Digital up Converter is a digital circuit which implements the conversion of a complex digital base band signal to a real pass band signal. The input complex base band signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The base band signal is filtered and converted to a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DUC typically performs pulse shaping and modulation of an intermediate carrier frequency appropriate for driving a final analog up converter and is used extensively in wireless and wire line communication systems.

A DUC consists of a series of cascaded interpolation finite impulse response (FIR) filters, a mixer, and a direct digital synthesizer (DDS). These filters are designed using Matlab and developed Verilog code. Simulation is performed using ModelSim and functional verification is carried out using Xilinx ISE and, FPGA implementation on Virtex-II Pro.

The DUC in this paper is a cascade of two FIR, Interpolation Filters and one Cascaded Integrator Comb (CIC) Interpolation Filter. The first FIR Interpolation Filter is a pulse shaping FIR filter that increases the sampling rate by 2 and performs transmitter Nyquist pulse shaping. The second FIR Interpolation Filter is a compensation FIR filter that increases the sampling rate by 2 and compensates for the distortion of the following CIC filter. The CIC Interpolation Filter is a programmable filter increases the sampling rate by 4 to 1448. Mixer is designed with an area efficient high-speed algorithm for variable multiplication and generation of carrier waves with a wide range of frequencies from the Direct Digital Synthesizer. Power consumed in this design is 103mWatts and the maximum frequency is up to 299.837 MHz.

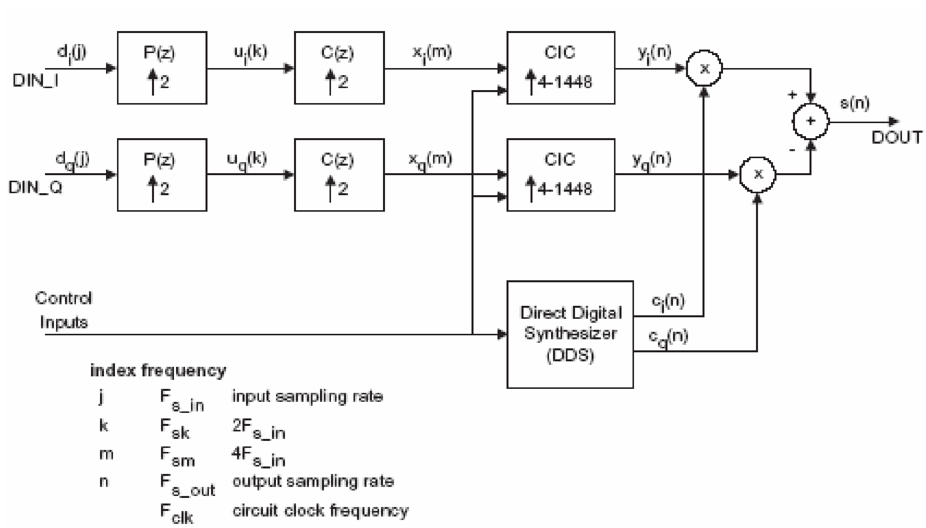
Keywords: FPGA, Down converter, Power line communication, FIR, Low Power, High Speed

1. Introduction

The Digital up Converter is a digital circuit which implements the conversion of a complex digital baseband signal to a real passband signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The baseband signal is filtered and converted to a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DUC typically performs pulse shaping and modulation of an intermediate carrier frequency appropriate for driving a final analog up converter and is used extensively in wireless and wire line communication systems.

2. Description of DUC

Figure 1: Digital up Converter Block diagram [1]



A block diagram of the Digital up Converter is shown in Figure 1. Spectral shaping of the complex input signal is performed by the PFIR filter. Typically this filter would be performing a Nyquist transmit filter operation with a rate-change of 2. Bias-free convergent rounding or truncation is employed between each processing stage to limit the bit growth through the DUC. Output from each of the PFIR filters is input to each of the CFIR filters, which is used to compensate for the droop within the CIC filter and performs the second rate-change. The CFIR also performs a rate-change of 2. The CFIR filter's output drives the input to the interpolating CIC filter, which is used for high sample rate change of 4.

The complex data stream from the CIC filter is mixed with a local oscillator generated by the DDS. Results from the mixers are combined, forming the final DUC result. The DUC result is often used as the input to a digital-to-analog converter (DAC) to generate an intermediate frequency analog signal. When the programmable CIC rate change option is selected, and the current rate change is less than the maximum rate change, then the output from the DUC will have times when VOUT is not valid and the last valid output data will be maintained on the DOUT port.

The DUC consists of following blocks

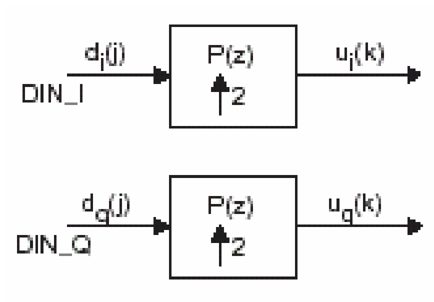
- Pulse shaping FIR filter
- Compensation FIR filter

- Cascaded Integrator Comb (CIC) filter
- Direct Digital Synthesizer (DDS)
- Multiplier

2.1. Pulse Shaping Fir Filter in DUC

Pulse Shaping FIR filter P (z) provides a sampling rate increase of 2 as shown in figure 2, and typically performs transmitter Nyquist pulse shaping. The programmable finite impulse response (PFIR) filter usually performs spectral shaping.

Figure 2: Block diagram of Pulse shaping block in DUC [1]



2.1.1. Description

FIR filters P(z) operate on the sequences di(j) and dq(j) applied to the DUC input ports DIN_I and DIN_Q. The sequences di(j) and dq(j) are up sampled by a factor of 2 by filtering with the Pulse Shaping Filter coefficients p(k), with the resulting sequences u(k) sampled at a rate of Fsk = 2Fs_in [1].

The pulse shaping finite impulse response filter P(z) typically conditions the transmitter signal's channel response and inter-symbol interference characteristics. Pulse shaping techniques are intended to decrease the profile of the transmitted signal, without compromising its information bearing properties, so that all the system creates less overall interference with one another.

The CFIR and PFIR are polyphase multirate filter structures that interpolate by a factor of 2, 4, or 8. The filter length for each filter is configurable from 4 to 1024 taps. The coefficient precision may also be customized and ranges from 4 to 32 bits [1].

The compensation finite impulse response (CFIR) filter is used to compensate for the droop in the passband of the CIC filter.

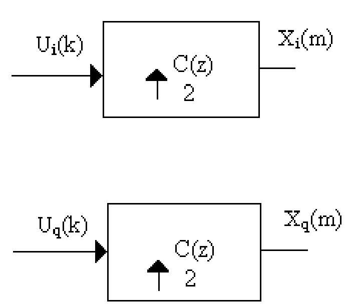
2.2. Compensation Filter

Compensation filter is a type of FIR filter used to compensate for loses in cascaded integrator comb(CIC) filter in the typical decimation/interpolation filtering applications a reasonably flat pass band and narrow transition region filter performance is required. These desirable properties are not provided by the CIC filters alone, with their drooping pass band gains.

2.2.1 Description

Compensation filter C(z) provides a sampling rate increases of 2 (interpolation) as shown in figure3, and filter is intended to compensate for the roll-off in the pass-band of the 3rd stage CIC filter. Typically, the C(z) will have a wide transition band to minimize the filter length. The coefficients needed to compensate for the CIC roll-off depend on the number of comb (differentiator) stages implemented in the CIC filter. The coefficients used here implements a 21-tap filter designed to compensate for a 5-stage CIC filter. If the CIC is to be configured with a different number of stages, and compensation is desired, then a new set must be generated for the compensation filter.

Figure 3: Compensation filter block in DUC sequence U(k) up-sampled factor 2 [1].



Two identical FIR filters C(z) operate on the sequence Ui(k) – the inphase component and Uq(k) – the quadrature phase component output from the pulse shaping filters. The compensation filter used here up-samples the input samples by a factor 2 and then output is passed through an FIR filter where the samples are convoluted by set of filter coefficients

2.3. Cascaded Integrator Comb (CIC) Filters

Cascaded integrator-comb, also called Hogenauer filters, are multi-rate filters that are used for realizing large sample rate conversions in digital systems. The main advantage of this filter is it does not use multipliers, and consists of only adders, subtractors and registers [2]. They are typically employed in applications that have a large excess sample rate. That is the system sample rate is much larger than the bandwidth occupied by the signal. CIC filters find application in

- Digital up-converters and digital down-converters.
- Channelization functions in a digital radio or MODEM
- For ultra-tight integration of GPS/INS/PL sensors
- Any filter structure that is required to efficiently effect a large sample rate change.

Characteristics of CIC Filters [3]

- Linear phase response;
- Utilize only delay and sum block (no multiplication);
- The integrator and comb structure are independent of rate changes (there is no need to reproject the filter on decimation/interpolation rate change).

2.3.1 CIC Interpolator

A CIC interpolation filter, as shown in figure 4, has two major sections: a comb section, which is a cascade of N combs and an integrator section, which is a cascade of N integrators. There is an interpolator or rate expansion switch (change by a factor R) between the two filter sections. The rate change switch is also known as a zero-stuffer as it pads zeros. The interpolator up samples the output of the last comb stage increasing the sample rate from fs/R to fs. One of the distinguishing factors of CIC filters is, the sampling rate of Comb filters is different from sampling rate of integrator, and i.e. the comb runs at a lower sampling frequency, which makes it easily programmable. Figure 5 gives a detailed structure of a CIC interpolator for 8 stages.

Figure 4: CIC Interpolator Structures [3]

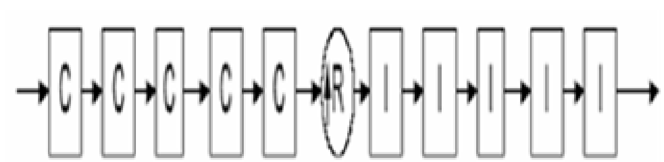
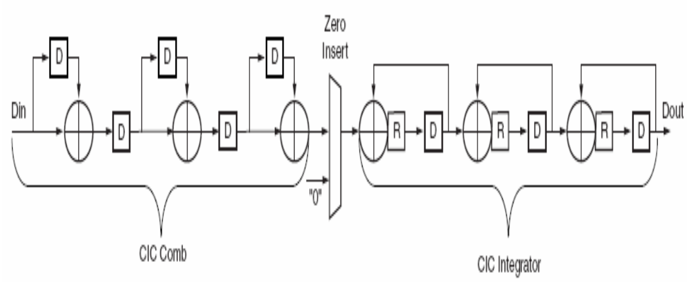


Figure 5: CIC Filter Structure Block Diagram [3]



2.3.2. Comb

A comb filter running at a low sampling rate fs/R, for a rate change of R is an odd symmetric filter described by

$Y[n] = x[n]-x[n-RM]$ (1)

In the equation, M is a design parameter and is known as differential delay. M is usually limited to 1 or 2. The corresponding transfer function at fs is

$Hc(z) = 1-z^{-RM}$ (2)

The comb sections are combined with a rate changer. Using a technique for multirate analysis of LTI systems the comb sections can be pushed through the rate changer and then become

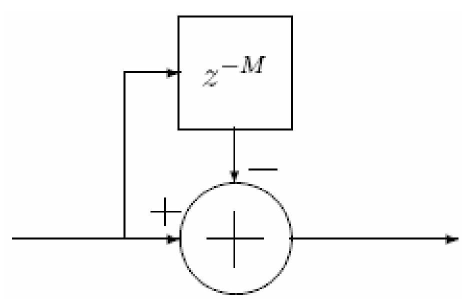
$Y[n] = x[n]-x[n-M]$ (3)

By this three things are achieved [3]:

1. Half of the filter has been slowed down and therefore efficiency is increased.
2. The numbers of delay elements required in the comb section have been reduced.
3. The integrator and comb stages are independent of rate changer.

The basic structure of a comb is as shown in figure 6

Figure 6: Basic Comb [3]



2.3.3. Integrator

An integrator is a single pole IIR filter with a unity feedback coefficient given by

$Y[n] = y[n-1]+x[n]$ (4)

The transfer function for an integrator on the z-plane is

$H_I(z) = 1/(1-z^{-1})$ (5)

The basic structure of an integrator is as shown in figure 7.

Figure 7: Basic Integrator [3]

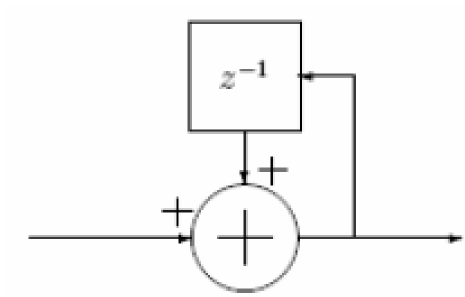
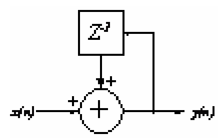
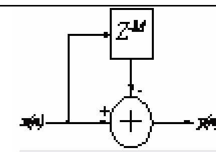


Table 1: Structure and Characteristics of Comb and Integrator [2]

Items	**Integrator**	**Comb**
Structure		
Sampling Rate	f_s	f_s / R
y[n]	y[n-1] + x[n]	x[n] – x[n-RM]
$H_I(z)$	$\frac{1}{1-z^{-1}}$	$1-z^{-RM}$
$\lvert H(e^{j\omega})\rvert^2$	$\frac{1}{2(1-\cos\omega)}$	$2(1-\cos RM\omega)$

This comparison table 1 tells about the difference between Comb and Integrator stages in CIC filter. These are derived in the above equations.

2.3.4. Frequency Characteristics

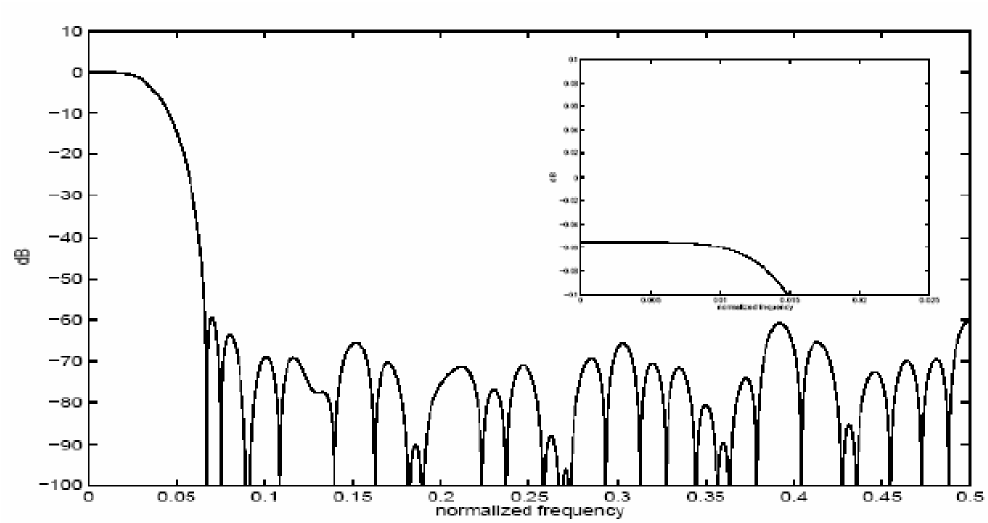
The transfer function for a CIC filter at fs is

$$H(z) = H_I^N(z)\, HC^N(z) \quad (6)$$

$$H(z) = (1 - z^{-RM})^N / (1 - z^{-1})^N \quad (7)$$

This equation shows that even though a CIC has integrators in it, which by themselves have an infinite impulse response a CIC filter is equal to cascade of an N FIR filters, each having a rectangular impulse response with unit coefficients. The frequency response of a CIC interpolator for an interpolation factor of 3 is as shown in figure 8.

Figure 8: CIC frequency response with interpolation ratio = 3 [4]



2.3.5. Implementation Details

The CIC designed for the DUC consists of the following features

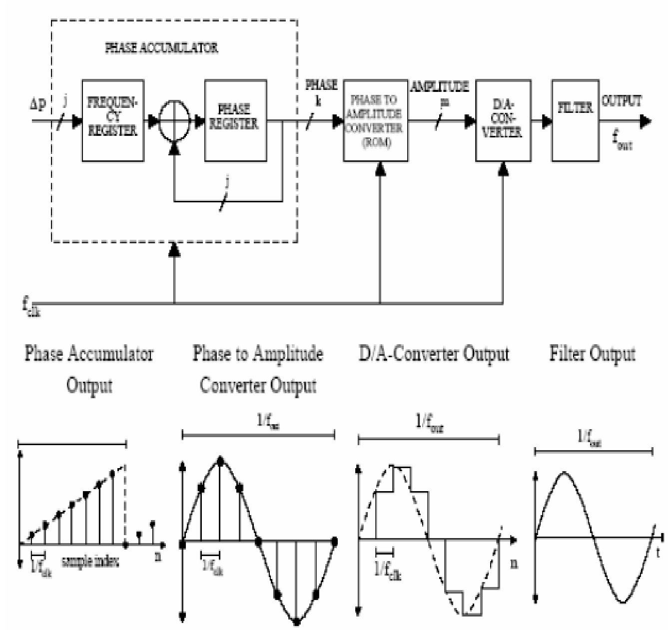
- 5 stage comb section and a 5 stage integrator section.
- Rate changer with an interpolation factor of 4.
- The number of comb and integrator stages is programmable.

2.4. Direct Digital Synthesizer

A Direct Digital Synthesizer (DDS) also known as Numerically Controlled oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It is an established method of generated periodic sinusoid signals whenever high frequency resolution, fast changes in frequency and phase, and high spectral purity of the output signal is required. A major advantage of the DDS is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly hop between frequencies [5].

2.4.1 Theory of Operation

Figure 9: DDS block diagram with DAC and filter [5]

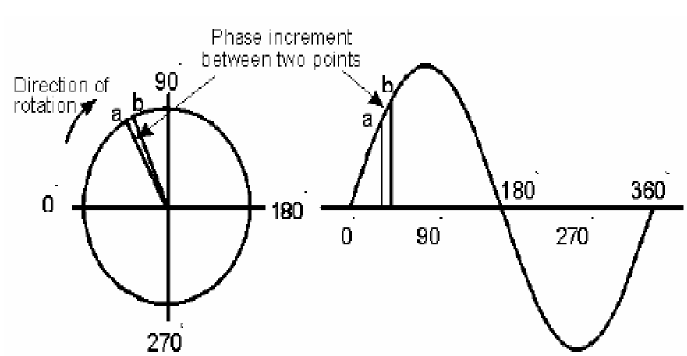


A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the synthesizer completes one waveform then determines the frequency [5], [6]. The basic block diagram of a DDS is as shown in Figure 9. The implementation of the DDS can be divide into two distinct parts namely the phase accumulator (phase generator) and the phase to amplitude converter.

a. Phase Accumulator

The phase accumulator shown consists of a j-bit frequency register which stores a digital phase increment value p followed by a j – bit full adder and a phase register. The phase increment value is entered into the frequency register. The operation of the phase accumulator can be considered by looking at the phase advances around a circle as shown in Figure 10. As the phase advances around the circle this corresponds to advances in the waveform, i.e. the greater the number corresponding to the phase, the greater the point is along the waveform [6]. By successively advancing the number corresponding to the phase it is possible to move further along the waveform cycle.

Figure 10: Operation of phase accumulator [6]



b. Phase to Amplitude Converter

Once the phase has been determined, it is necessary to convert this into a digital representation of the waveform. This is accomplished using a phase to waveform converter. This is a memory that stores a number corresponding to the voltage required for each value of phase on the waveform. The memory is either a read only memory (ROM) or programmable read only memory (PROM). This contains a vast number of points on the waveform. A very large number of points are required so that the phase accumulator can increment by a certain number of points to set the required frequency [5].

The output of the DDS is usually given to a DAC and then filtered to any unwanted signals. Phase quantization can be achieved in the DDS by truncating the phase information accumulator. Phase quantization is done to keep the memory requirements of the phase to waveform converter low. But it produces unwanted spurious spectral components in the DDS output signals, know as spurs. Also sometimes images of the signals are generated on either side of the clock frequency and its multiples. These can be removed by low pass filtering.

2.4.2 Performance Details of DDS

- For the implementation of DDS consider the phase of the accumulator to be ‘k’ bits and assume that the period of the output signal is 2Πrad. Then the maximum phase is represented by the number 2^k.
- $\triangle$p denotes the phase increment related to the output frequency f_{ou}t. It is an integer number with k-1 bits. During one sample period increases by $\triangle$p and so the output frequency to reach the maximum phase 2N is given by

$$f_{out} = f_s \triangle p / 2^k \text{ Hz} \quad (8)$$

The tuning step $\triangle f_{out}$ min that is the smallest step in frequency that the DDS can achieve is given by

$$\triangle f_{out} \min = f_s/2^k \quad (9)$$

This is also the minimum frequency that the DDS can generate with $\triangle p = 1$ i.e. the smallest phase increment which still increases the phase. Thus, the minimum frequency resolution is attained by the total number of bits available in the phase accumulator.

2.4.3. DDS Implementation Details

The DDS designed for the Digital up Converter consists of the following features

- It is a quadrature output DDS which synthesizes both sine and cosine waves.
- A look-up table or ROM where all the phase values of the sine wave or cosine wave are stored. 1024 values are used to represent the sine or cosine wave.
- The values stored represent one quadrant of the output wave. The entire sine or cosine wave is stimulated using their symmetrical property.
- One phase value is synthesized on every clock pulse.
- Phase increment can be obtained in steps of 1 to 1024.

Advantages of DDS

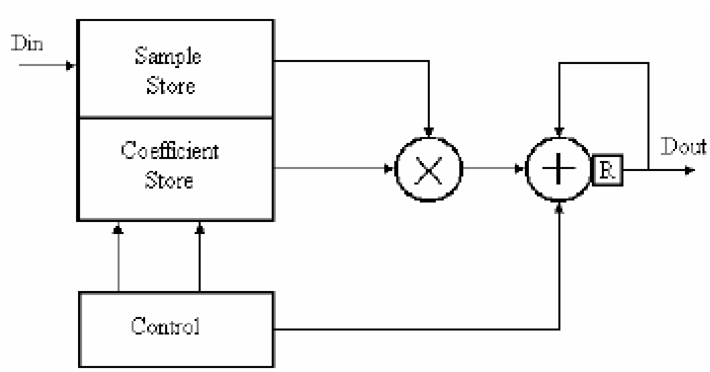
Today’s cost-competitive, high-performance, functionally integrated DDS ICs are becoming common in both communication systems and sensor applications. The advantages that make them attractive to design engineers include [7]:

- Digitally controlled micro-hertz frequency-tuning and sub-degree phase-tuning capability,
- Extremely fast hopping speed in tuning output frequency (or phase); phase-continuous frequency hops with no overshoot/undershoot or analog-related loop settling-time anomalies,
- The digital architecture of DDS eliminates the need for the manual tuning and tweaking related to component aging and temperature drift in analog synthesizer solutions, and
- The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled and optimized with high resolution under processor control.

2.5 Multiply Accumulator

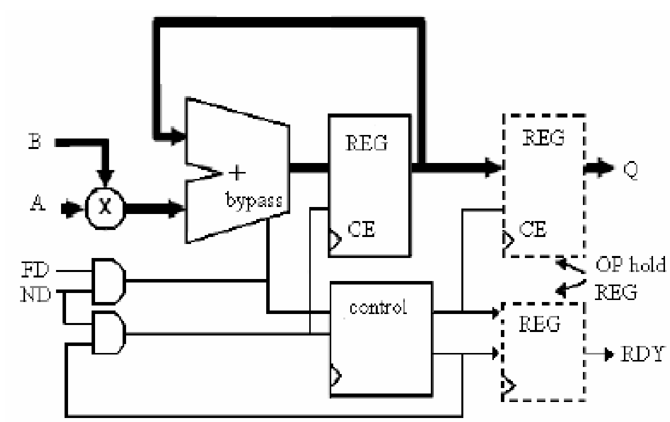
MAC is a parallel multiply-accumulator module. FIR filters typically are implemented in Xilinx FPGAs using either the MAC implementation or the DA (Distributed Arithmetic) technique. MAC based implementation is used here in the DUC FIR filters implementations. Figure 11 shows a MAC FIR filter simplified block diagram.

Figure 11: Simplified Block diagram of MAC [8]



2.4.1 Discription

Figure 12: Detailed MAC Block Diagram [8]



The MAC based architecture uses a multiplier to perform the tap product calculations, followed by an accumulator to perform the filter addition operations.

Figure 12 shows a detailed block diagram of a MAC. A and B are two n-bit inputs, FD (first data) and ND (new data) are two control signals used. Q is the output of MAC; RDY is an output signal that indicates that a valid output is present at Q. Registers is used for temporary storage of data during operation.

The overall of MAC is given by

$$\sum_{n=0}^{count-1} (\pm 1) * A(n) * B(n) \qquad (10)$$

2.5.2. Advantages of MAC

The advantages of MAC over the distributed Arithmetic technique

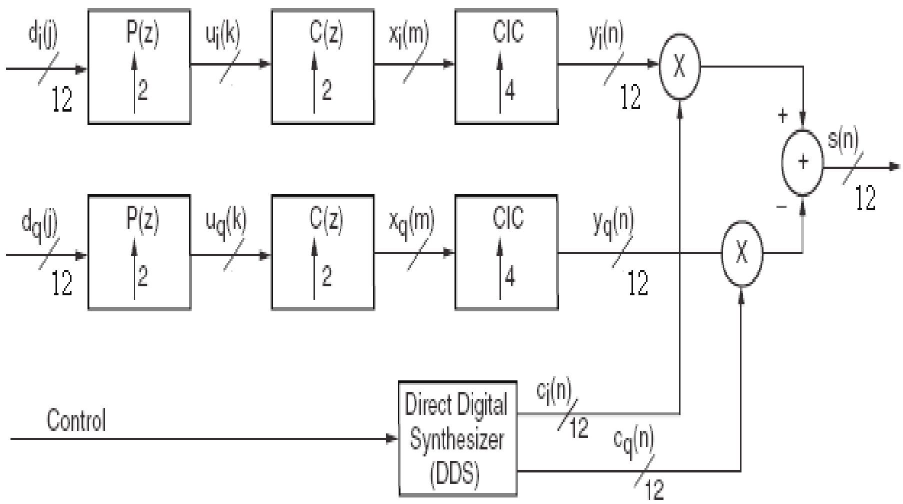
- MAC uses much less memory than DA which has a heavy use of look-up tables

- When a filter operation rate exceeds that of a single MAC, multiple MACs can be placed in parallel, and the individual results than added to form the final filter result.

3.0. Results and Discussions

Digital Up Converter (DUC) was developed in Verilog code using Xilinx ISE tool. The code was simulated in ModelSim tool.

Figure 13: Discussing Results on Digital Up Converter



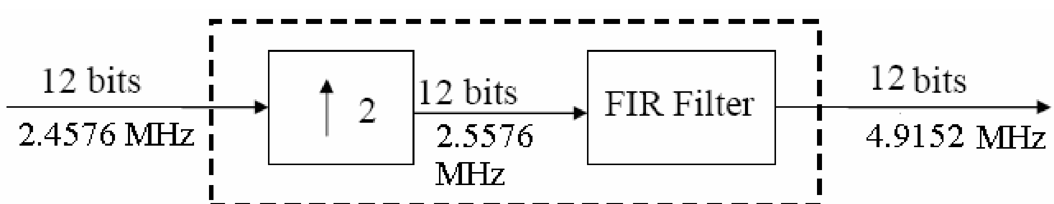
index		frequency
j	Fs_in	2.4576 MHz
k	Fsk	4.9152 MHz
m	Fsm	9.8304 MHz
n	Fs_out	39.3216 MHz

3.1. Pulse Shaping Filter P(Z)

The first filtering stage P(z) is a low-pass filter that performs interpolating by a sampling factor 2. This filter is a 32-tab finite impulse response (FIR) filter. As shown in the figure 13 di(j) and dq(j) are the inputs to P(z). Those inputs are taken from Matlab. 1024 samples are taken and giving it to Pulse shaping filter P(z). These samples are stored in to RAM and written the Verilog code. Internally Pulse shaping filter has a MAC unit.

The P(z) stage is a real filter operating on a complex input signal d(j), such two identical 12-tap FIR filtering operations are performed on the input frequency, so that the complex output signal x(m) is sampled at 2.4576 MHz. the P(z) filter also provides a 1:2 sampling rate increase from the chip rate F_{s_in} to F_{sk} i.e. the output frequency of the PFIR is 4.9152 MHz as shown in figure 14.

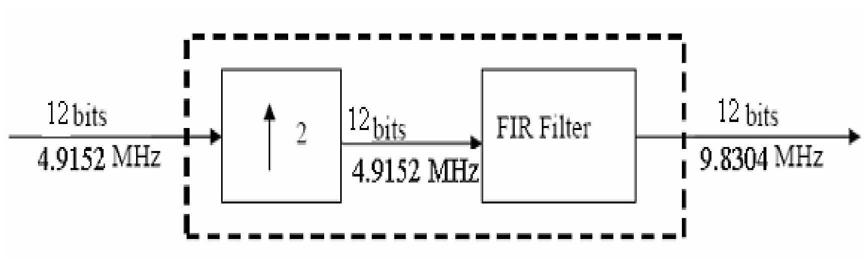
Figure 14: PFIR used in DUC



3.2. Compensation Filter C(z)

The second filtering stage is C(z), internally the C(z) has a MAC unit. The output of PFIR or P(z) is given to CFIR or C(z). The C(z) stage is a real filter operating on a complex input signal u(k) as shown in figure 13. FIR filtering operations are performed on the input signal components $u_i(k)$ and uq(k). The filter C(z) increases the sampling rate by a factor of 2, so that the complex output signal x(m) is sampled at 9.8304 MHz frequency as shown in figure 15. The Compensation filter CFIR operates on lower sampling rate of the signal as compared to the CIC filter that operates at a higher sampling rate.

Figure 15: Compensation Filter Output

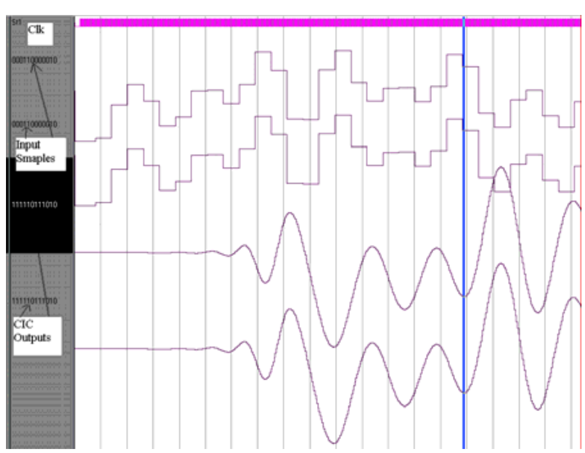


3.3. CIC Filter

CIC filter is the last stage of the interpolation filtering. The CIC filters use no multipliers. They use only adders, subtractors, and registers. The C(z) output is given to CIC as an input. The CIC interpolation filter is composed of a series of N differentiators (the Comb section) followed by a series of N integrators. The differentiators run at the filter input signal sampling rate F_{sm}, permitting the sharing of a single subtraction circuit among the 2N differentiators of the I and Q filters. CIC filter increases the sample rate by a factor 4. The output frequency yi(n) is 39.3216 MHz.

The input given to the filter was a sine wave of 1024 samples of width 12 bits which is a top wave shown in figure 16. Output from the block was a recovered sine wave as expected that was up sampled by a factor of 4. Output of the filter has a high gain contributed by the CIC filter. The output of the CIC filter was multiplied with DDS to give the final products that were then summed to give the result.

Figure 16.: Simulation output of CIC filter

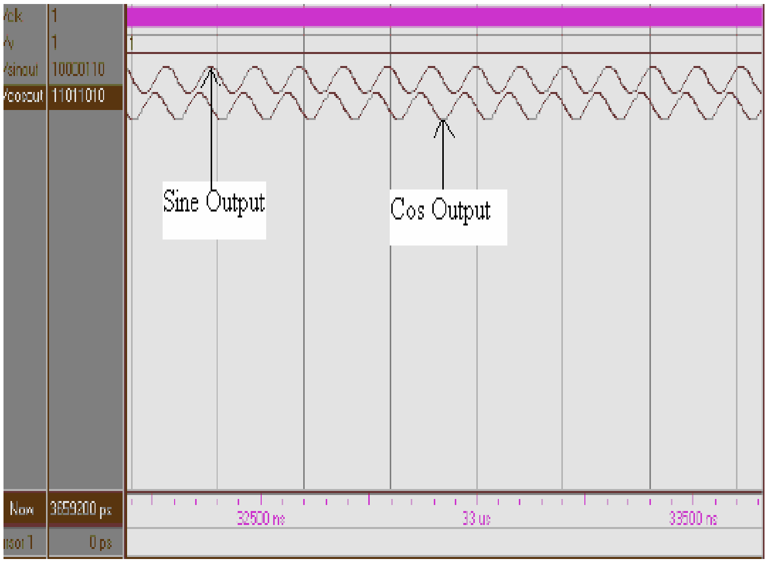


3.4. Direct Digital Synthesizer

DDS is a method of producing an analog waveform usually a sine wave, by generating a time varying signal in digital from and then performing a digital-to-analog conversion.

To generate a periodic waveform, the circuit is set up so that one pass through the table takes a time equal to the period of the waveform. The reference frequency is 1 MHz, and the table contains 1000 entries, then a complete pass through the table with a phase increment of 1 will take 1000 / 1 MHz = 1 ms, so the frequency of the output waveform will be 1/(1 ms) = 1 kHz as shown in figure 17.

Figure 17: Simulation waveform of DDS



3.6. Simulation of Digital Up Converter

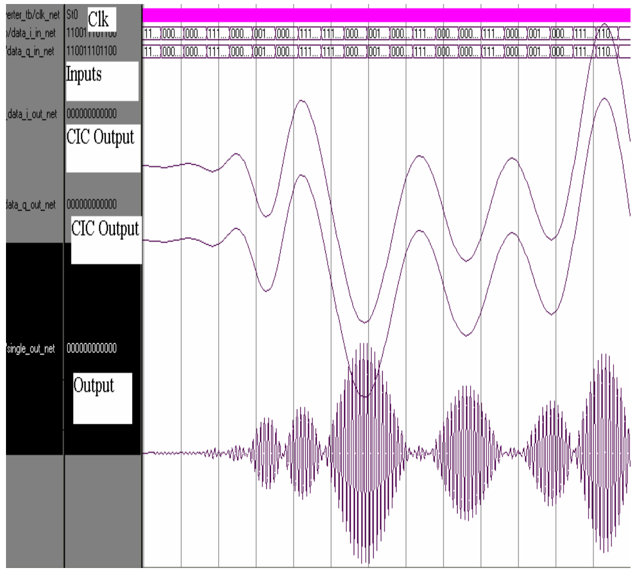
The output of CIC and DDS are giving it to mixer. Here the Booth's multiplier was developed.

Booths Multiplier

- Encoding scheme to reduce number of stages in multiplication.
- Performs two bits of multiplication at once – requires half the stages.
- Each stage is slightly more complex than simple multiplier, but adder/subtractor is almost as small/fast as adder.

Results for the multiplication were validated for two 12-bit operands. When both the operands are positive the product is a positive product. If any one of the operands changes signs the product becomes negative indicating signed multiplication. The case where both operands are negative giving a positive value for the product further proves the concept that the multiplier is a signed multiplier. The multiplier is validated for operands in 2's complement notation. The multiplier block used in the project had to multiply the input two 12-bit data to give a 24-bit output. Both multipliers are added that result is the Digital Up Converter as shown in figure 18.

Figure 18: Simulation Output of Digital up Converter

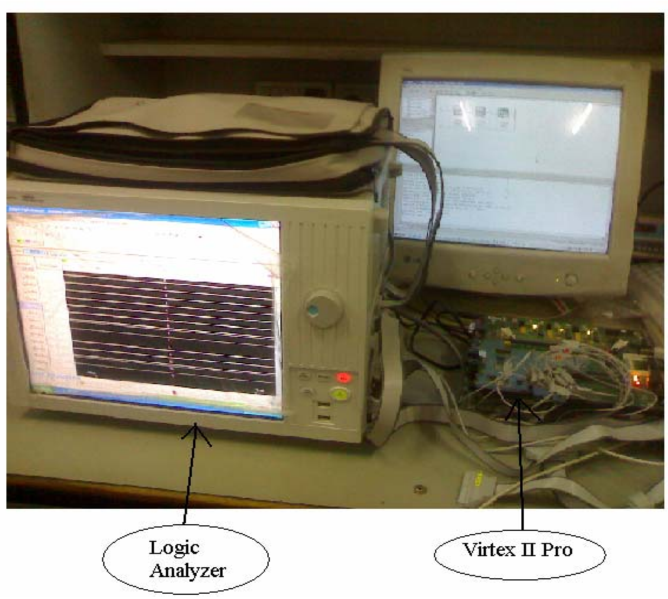


The conversion of the filtered base band complex signal, y(n) = yi(n)+yq(n), to an intermediate frequency is accomplished using a DDS, two multipliers, and a subtractor circuit. The DDS outputs a complex sinusoid, c(n) = ci(n)+cq(n), which is mixed with y(n) to produce the real DUC output signal s(n). The simulation output of Digital up converter is as shown in figure 18. The output frequency of Digital up Converter is 39.3216 MHz.

3.7. FPGA Implementation of DUC

After synthesis is done coming to FPGA implementation. For the FPGA implementation Virtex II pro broad and the logic analyzers are used. The logic analyzer is used to see the output wave from in digital format as shown in figure 19.

Figure 19: FPGA Implementation



Field Programmable Gate Arrays (FPGAs) are the leading implementation path for reprogrammable, high performance applications like Digital Signal Processing (DSP).

4. Conclusions and Recommendations for Future Work

4.1. Conclusion

This paper deals with the development of a Digital Up Converter for Power Line Communication Systems equipment. The base band signal that is received by the equipment is in the 0 – 4 KHz range. The carrier signal frequency used to modulate the signal lies between 20 KHz – 512 KHz. DUC block was developed to retrieve the signal.

In this design 3 individual interpolation filters were cascaded along with a DDS and a mixer into a digital up converter. Coding of the sub-blocks of the main DUC has been implemented using Verilog. Simulations were carried out for the coded blocks and the results have been verified. The output was simulated using ModelSim, and it is synthesized using Xilinx ISE and the results for the interpolation filters were verified using MATLAB. Verilog code is implemented using FPGA Virtex II Pro.

In the course of doing the project, insight knowledge has been gained into various fields like

- The Virtex II Pro FPGA architecture.
- Coding using Verilog.
- Digital signal processing concepts.
- Network and communication concepts.
- Tools such as Xilinx ISE, ModelSim, Matlab and Xilinx system generator.

Table 2: Frequency Comparison in different stages in DUC

Stages	Sampling factor	Frequency
PFIR	2	4.9152 MHz
CFIR	2	9.8304 MHz
CIC Filter	4	39.16 MHz

DUC has 3 different interpolator stages as written in table 2. The first stage of interpolator is PFIR, in this up sampled by a factor 2. Input frequency is 2.4576 MHz and the output frequency of PFIR is 4.9152 MHz. The second stage is CFIR filter, it is upsampled by a factor 2 and the output frequency is 9.8304 MHz. The third stage interpolator is CIC interpolating filter with a sampling factor 4, and then the output frequency of the DUC is 39.16 MHz.

Power Statistics

Power Consumed by the Digital Up Converter designed is 103mWatts and the maximum frequency is 299.837 MHz as shown in table 3. The above given statistics are obtained on synthesizing the Verilog code written for DUC and it can be implemented on FPGA using 50% of resources further it can be improved.

Table 3: Comparison of paper and the result obtained

Parameters	Paper	Results Obtained
Power	200mWatts	103mWatts
Maximum Frequency	200 MHz	299.837MHz

4.2. Recommendations for Further Work

- The designed code requires hardware with more resources as it exceeds the capacity of lower FPGA devices. The hardware can be minimized by designing the code in such a way that the memory used is less in comparison with the existing one. This also improves the frequency of operation.

- We can use as an IP core.

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